Notice of References Cited Application/Control No. 09/879,197 Examiner Fred Ferris Applicant(s)/Patent Under Reexamination KOMODA ET AL. Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-6,557,150 B1	04-2003	Honmura et al.	716/6
	В	US-6,473,725 B1	10-2002	Schoellkopf et al.	703/15
	С	US-6,028,995 A	02-2000	Jetton et al.	703/19
	D	US-5,838,947 A	11-1998	Sarin, Harish K.	703/14
	Е	US-5,274,568 A	12-1993	Blinne et al.	716/6
	F	US-			
	G	US-			
	Н	US-			
	1	US-			
	J	US-			
	к	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р			•		
	D					
	R					
	S					
	Т					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)				
	U					
	V	п				
	w	"Efficent Gate Delay Modeling for Large Interconnect Loads", A.B. Kahng et al, IEEE 0-8186-7286-2/96, IEEE 1996				
	х	"Transistor-Level Estimation of worst-Case Delay in MOS VLSI Circuits", M.R. Dagenais, IEEE Transactions on Computer Aided Design, Vol. II, No. 3, March 1992				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.